

## Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection

August 1997

### Features

- Analog Overvoltage Protection . . . . . 70V<sub>P-P</sub>
- No Channel Interaction During Overvoltage
- Guaranteed r<sub>ON</sub> Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15V
- Access Time (Typical) . . . . . 500ns
- Standby Power (Typical) . . . . . 7.5mW

### Applications

- Data Acquisition
- Industrial Controls
- Telemetry

### Description

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed r<sub>ON</sub> matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant 70V<sub>P-P</sub> levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16-Channel, the HI-547 is an 8-Channel differential, the HI-548 is a single 8-Channel and the HI-549 is a 4-Channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-546 and HI-547 devices are available in a 28 lead Plastic or Ceramic DIP and a 28 pad Ceramic LCC package. The HI-548/549 devices are available in a 16 lead Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

The HI-546, HI-547, HI-548 and HI-549 are offered in industrial/commercial and military grades. Additional Hi-Rel screening including 160 hour Burn-In is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

### Ordering Information

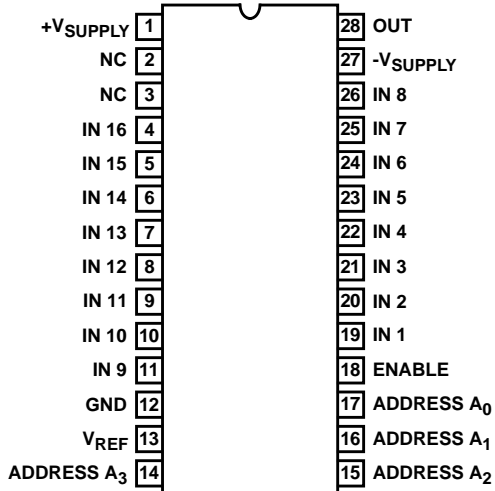
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0546-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0546-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0546-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0546/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0546-5	0 to 75	28 Ld PDIP	E28.6
HI3-0546-9	-40 to 85	28 Ld PDIP	E28.6
HI4-0546/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0546-5	0 to 75	28 Ld PLCC	N28.45
HI9P0546-5	0 to 75	28 Ld SOIC	M28.3
HI9P0546-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0547-2	-55 to 125	28 Ld CERDIP	F28.6
HI1-0547-4	-25 to 85	28 Ld CERDIP	F28.6
HI1-0547-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0547/883	-55 to 125	28 Ld CERDIP	F28.6
HI3-0547-5	0 to 75	28 Ld PDIP	E28.6
HI4-0547/883	-55 to 125	28 Ld CLCC	J28.A
HI4P0547-5	0 to 75	28 Ld PLCC	N28.45
HI9P0547-5	0 to 75	28 Ld SOIC	M28.3
HI9P0547-9	-40 to 85	28 Ld SOIC	M28.3

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1-0548-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0548-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0548-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0548/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0548-5	0 to 75	16 Ld PDIP	E16.3
HI4-0548/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0548-5	0 to 75	20 Ld PLCC	N20.35
HI9P0548-5	0 to 75	16 Ld SOIC	M16.15
HI9P0548-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0549-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0549-4	-25 to 85	16 Ld CERDIP	F16.3
HI1-0549-5	0 to 75	16 Ld CERDIP	F16.3
HI1-0549/883	-55 to 125	16 Ld CERDIP	F16.3
HI3-0549-5	0 to 75	16 Ld PDIP	E16.3
HI3-0549-9	-40 to 85	16 Ld PDIP	E16.3
HI4-0549/883	-55 to 125	20 Ld CLCC	J20.A
HI4P0549-5	0 to 75	20 Ld PLCC	N20.35
HI9P0549-5	0 to 75	16 Ld SOIC	M16.15
HI9P0549-9	-40 to 85	16 Ld SOIC	M16.15

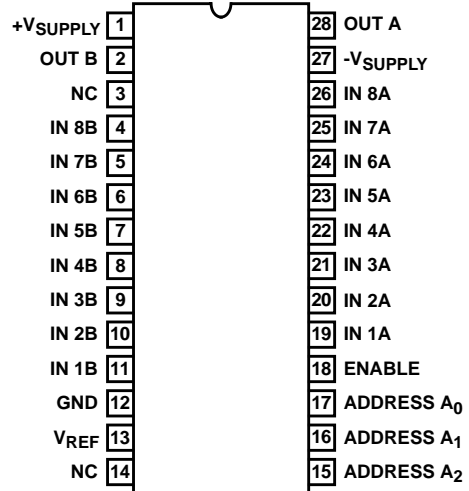
# HI-546, HI-547, HI-548, HI-549

## Pinouts

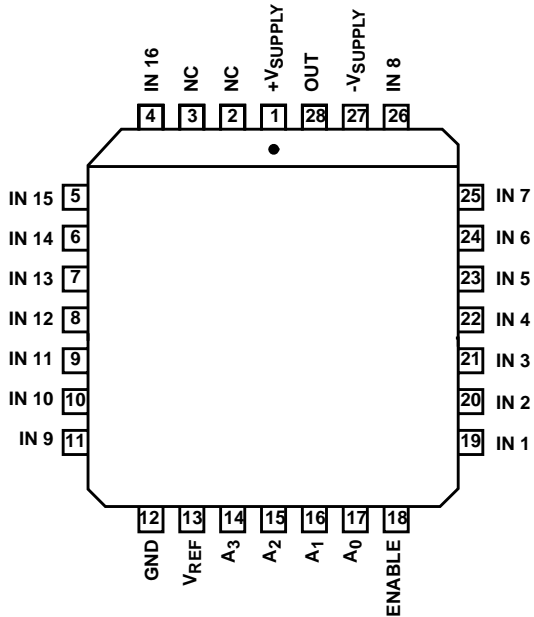
HI1-0546 (CERDIP), HI3-0546 (PDIP), HI9P0546 (SOIC)  
TOP VIEW



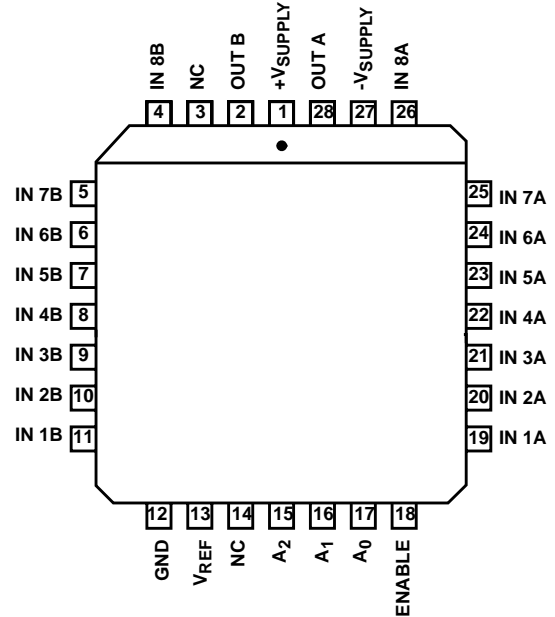
HI1-0547 (CERDIP), HI3-0547 (PDIP), HI9P0547 (SOIC)  
TOP VIEW



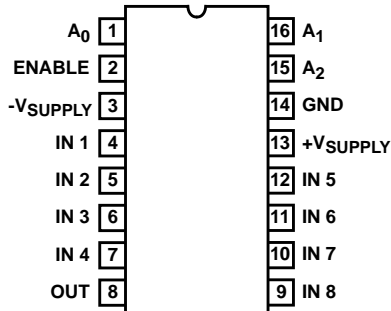
H14-0546 (CLCC)  
HI4P0546 (PLCC)  
TOP VIEW



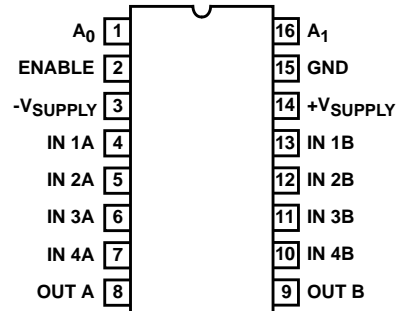
H14-0547 (CLCC)  
HI4P0547 (PLCC)  
TOP VIEW



HI1-0548 (CERDIP), HI3-0548 (PDIP), HI9P0548 (SOIC)  
TOP VIEW



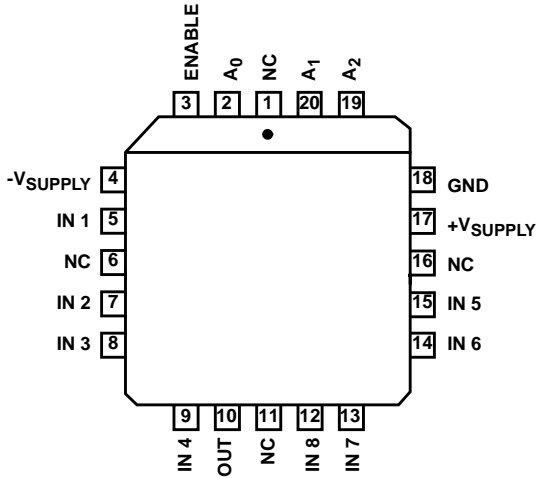
HI1-0549 (CERDIP), HI3-0549 (PDIP), HI9P0549 (SOIC)  
TOP VIEW



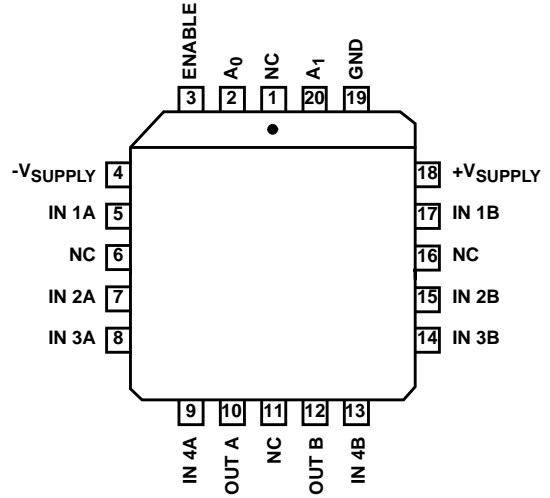
# HI-546, HI-547, HI-548, HI-549

## Pinouts (Continued)

HI14-0548 (CLCC)  
HI4P0548 (PLCC)  
TOP VIEW

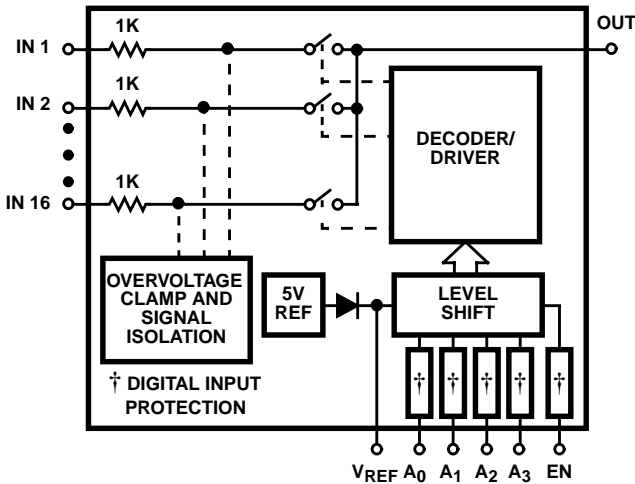


HI4-0549 (CLCC)  
HI4P0549 (PLCC)  
TOP VIEW

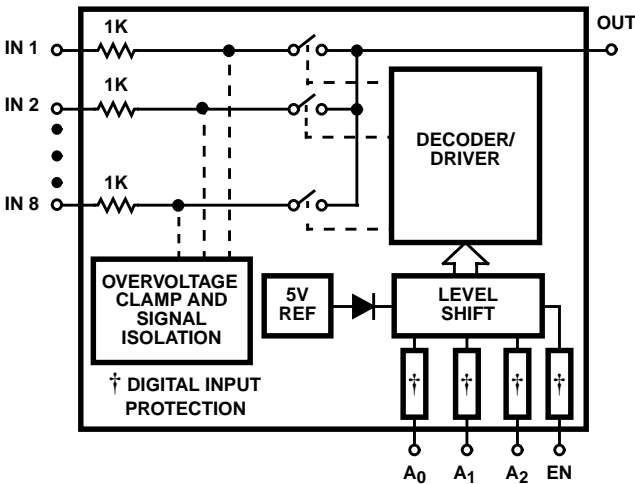


## Functional Diagrams

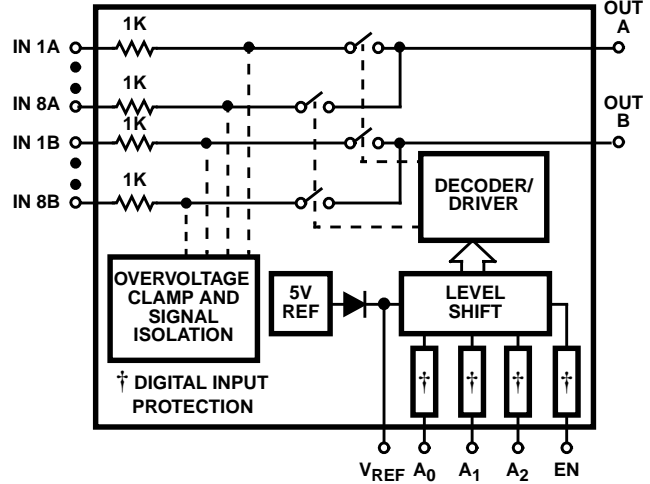
HI-546



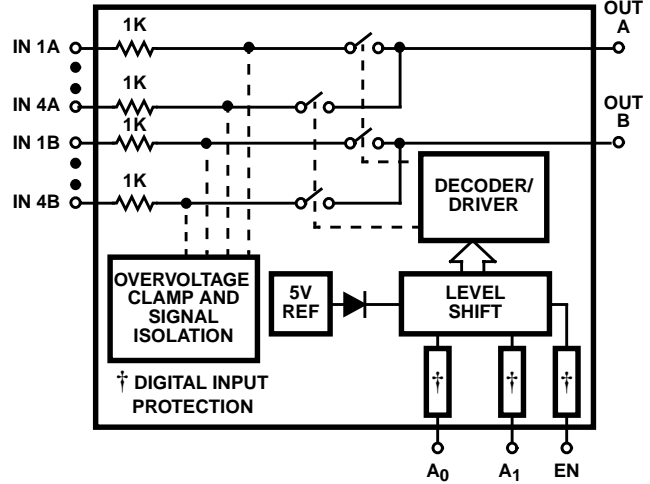
HI-548



HI-547

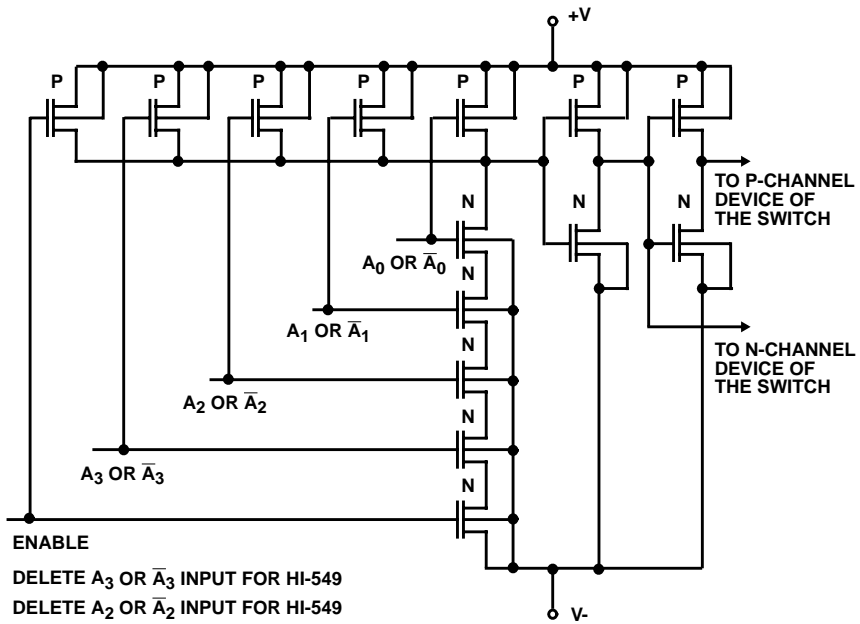


HI-549

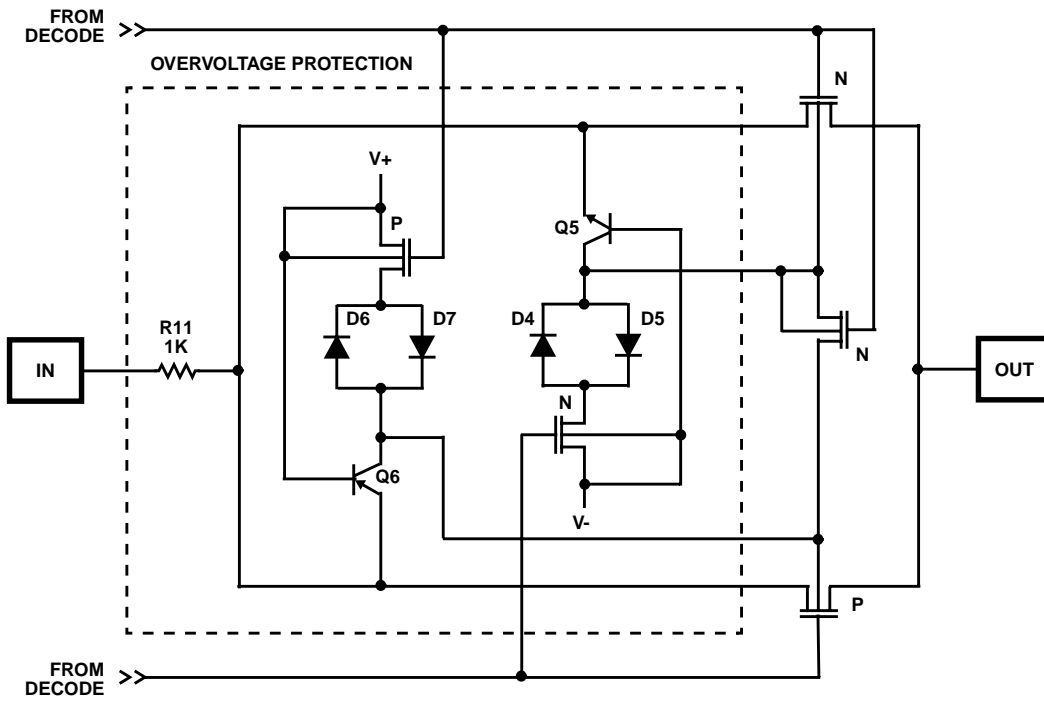


Schematic Diagrams

ADDRESS DECODER

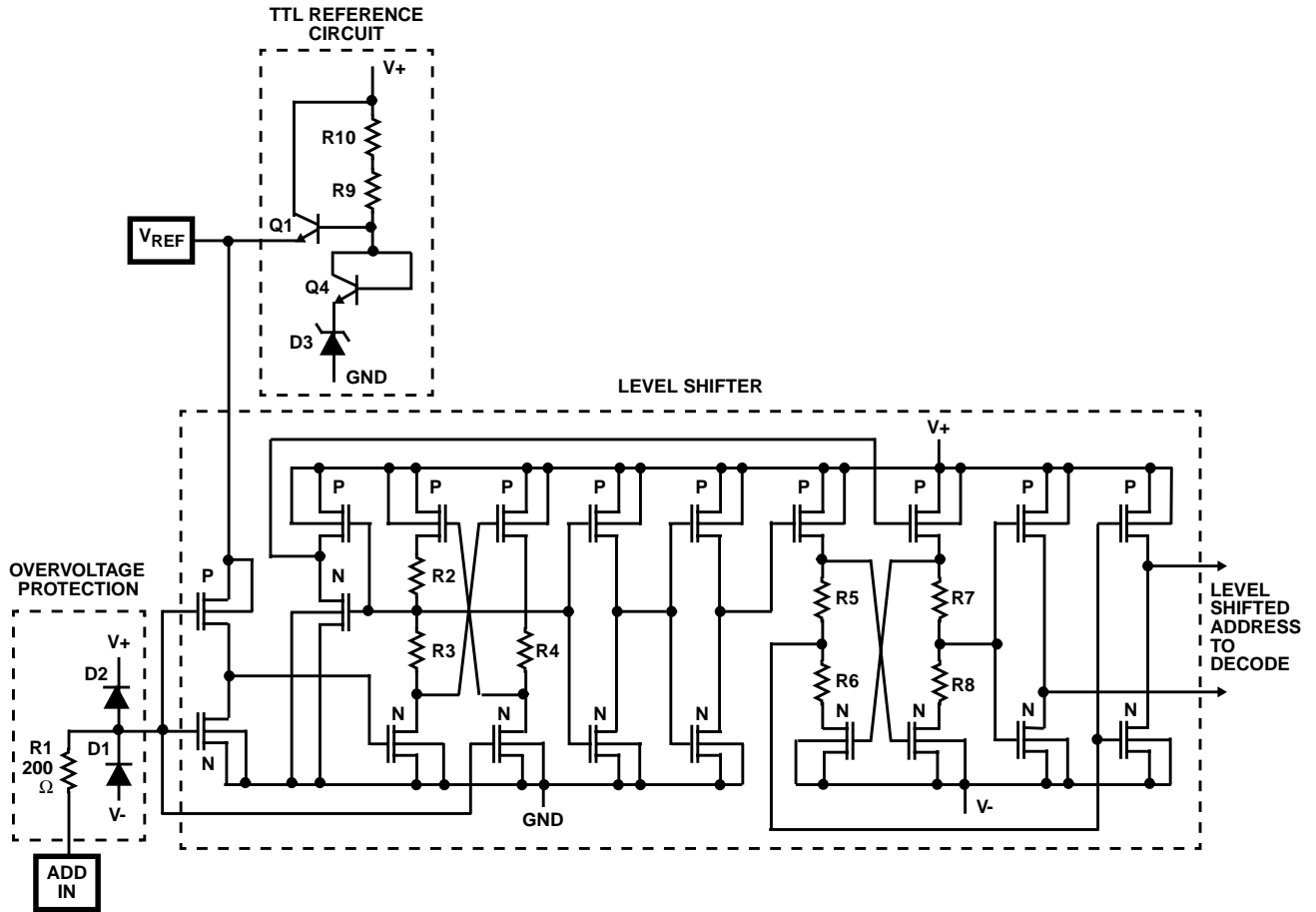


MULTIPLEX SWITCH



Schematic Diagrams (Continued)

ADDRESS INPUT BUFFER AND LEVEL SHIFTER



## HI-546, HI-547, HI-548, HI-549

### Absolute Maximum Ratings

V <sub>SUPPLY(+)</sub> to V <sub>SUPPLY(-)</sub> .....	+44V
V <sub>SUPPLY(+)</sub> to GND .....	+22V
V <sub>SUPPLY(-)</sub> to GND .....	-25V
Digital Input Overvoltage	
+V <sub>EN</sub> , +V <sub>A</sub> .....	+V <sub>SUPPLY</sub> +4V
-V <sub>EN</sub> , -V <sub>A</sub> .....	-V <sub>SUPPLY</sub> -4V
	or 20mA, Whichever Occurs First
Analog Signal Overvoltage (Note 6)	
+V <sub>S</sub> .....	+V <sub>SUPPLY</sub> +20V
-V <sub>S</sub> .....	-V <sub>SUPPLY</sub> -20V
Continuous Current, S or D .....	.20mA
Peak Current, S or D .....	.40mA
	(Pulsed at 1ms, 10% Duty Cycle Max)

### Operating Conditions

Operating Temperature Ranges	
HI-546/547/548/549-2 .....	-55°C to 125°C
HI-546/547/548/549-4 .....	-25°C to 85°C
HI-546/547/548/549-5 .....	.0°C to 75°C
HI-546/547/548/549-9 .....	-40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 Ld CERDIP Package .....	85	32
28 Ld CERDIP Package .....	55	18
20 Ld CLCC Package .....	80	28
28 Ld CLCC Package .....	70	20
28 Ld PDIP Package .....	60	N/A
16 Ld PDIP Package .....	100	N/A
28 Ld PLCC Package .....	70	N/A
20 Ld PLCC Package .....	80	N/A
28 Ld SOIC Package .....	70	N/A
16 Ld SOIC Package .....	100	N/A
Maximum Junction Temperature		
Ceramic Package .....		175°C
Plastic Package .....		150°C
Maximum Storage Temperature Range .....		-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....		300°C
		(PLCC, SOIC - Lead Tips Only)

**Electrical Specifications** Supplies = +15V, -15V; V<sub>REF</sub> Pin = Open; V<sub>AH</sub> (Logic Level High) = +4V; V<sub>AL</sub> (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>SWITCHING CHARACTERISTICS</b>									
Access Time, t <sub>A</sub>		25	-	0.5	-	-	0.5	-	μs
		Full	-	-	1.0	-	-	1.0	μs
Break-Before Make Delay, t <sub>OPEN</sub>		25	25	80	-	25	80	-	ns
Enable Delay (ON), t <sub>ON(EN)</sub>		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), t <sub>OFF(EN)</sub>		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time (0.1%) (0.01%)		25	-	1.2	-	-	1.2	-	μs
		25	-	3.5	-	-	3.5	-	μs
"Off Isolation"	Note 5	25	50	68	-	50	68	-	dB
Channel Input Capacitance, C <sub>S(OFF)</sub>		25	-	5	-	-	5	-	pF
Channel Output Capacitance C <sub>D(OFF)</sub>	HI-546	25	-	52	-	-	52	-	pF
	HI-547	25	-	30	-	-	30	-	pF
	HI-548	25	-	25	-	-	25	-	pF
	HI-549	25	-	12	-	-	12	-	pF
Input to Output Capacitance, C <sub>DS(OFF)</sub>		25	-	0.1	-	-	0.1	-	pF
<b>DIGITAL INPUT CHARACTERISTICS</b>									
Input Low Threshold, TTL Drive, V <sub>AL</sub>		Full	-	-	0.8	-	-	0.8	V

## HI-546, HI-547, HI-548, HI-549

**Electrical Specifications** Supplies = +15V, -15V; V<sub>REF</sub> Pin = Open; V<sub>AH</sub> (Logic Level High) = +4V; V<sub>AL</sub> (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HI-54X-2			HI-54X-4, -5, -9			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Input High Threshold, V <sub>AH</sub>	Note 7	Full	4.0	-	-	4.0	-	-	V	
MOS Drive (HI-546/547 Only), V <sub>AL</sub>	Note 8	25	-	-	0.8	-	-	0.8	V	
MOS Drive (HI-546/547 Only), V <sub>AH</sub>	Note 8	25	6.0	-	-	6.0	-	-	V	
Input Leakage Current (High or Low), I <sub>A</sub>	Note 4	Full	-	-	1.0	-	-	1.0	μA	
<b>ANALOG CHANNEL CHARACTERISTICS</b>										
Analog Signal Range, V <sub>S</sub>		Full	-15	-	+15	-15	-	+15	V	
On Resistance, r <sub>ON</sub>	Note 1	25	-	1.2	1.5	-	1.5	1.8	kΩ	
		Full	-	1.5	1.8	-	1.8	2.0	kΩ	
Δr <sub>ON</sub> , (Any Two Channels)		25	-	-	7.0	-	-	7.0	%	
Off Input Leakage Current, I <sub>S(OFF)</sub>	Note 2	25	-	0.03	-	-	0.03	-	nA	
		Full	-	-	50	-	-	50	nA	
Off Output Leakage Current, I <sub>D(OFF)</sub>	Note 2	25	-	0.1	-	-	0.1	-	nA	
		HI-546	Full	-	-	300	-	-	300	nA
		HI-547	Full	-	-	200	-	-	200	nA
		HI-548	Full	-	-	200	-	-	200	nA
		HI-549	Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, I <sub>D(OFF)</sub>	Note 3	25	-	4.0	-	-	4.0	-	nA	
		Full	-	-	2.0	-	-	-	μA	
On Channel Leakage Current, I <sub>D(ON)</sub>	Note 2	25	-	0.1	-	-	0.1	-	nA	
		HI-546	Full	-	-	300	-	-	300	nA
		HI-547	Full	-	-	200	-	-	200	nA
		HI-548	Full	-	-	200	-	-	200	nA
		HI-549	Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current (HI-547, HI-549 Only), I <sub>DIFF</sub>		Full	-	-	50	-	-	50	nA	
<b>POWER REQUIREMENTS</b>										
Power Dissipation, P <sub>D</sub>		Full	-	7.5	-	-	7.5	-	mW	
Current, I <sub>+</sub>	Note 6	Full	-	0.5	2.0	-	0.5	2.0	mA	
Current, I <sub>-</sub>	Note 6	Full	-	0.02	1.0	-	0.02	1.0	mA	

**NOTES:**

1. V<sub>OUT</sub> = ±10V, I<sub>OUT</sub> = ±100μA.
2. 10nA is the practical lower limit for high speed measurement in the production test environments.
3. Analog Overvoltage = ±33V.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V<sub>EN</sub> = 0.8V, R<sub>L</sub> = 1K, C<sub>L</sub> = 15pF, V<sub>S</sub> = 7V<sub>RMS</sub>, f = 100kHz.
6. V<sub>EN</sub>, V<sub>A</sub> = 0V or 4V.
7. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V<sub>SUPPLY</sub> are recommended.
8. V<sub>REF</sub> = +10V.

**Typical Performance Curves**  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = +4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$ ,  $V_{\text{REF}} = \text{Open}$ , Unless Otherwise Specified

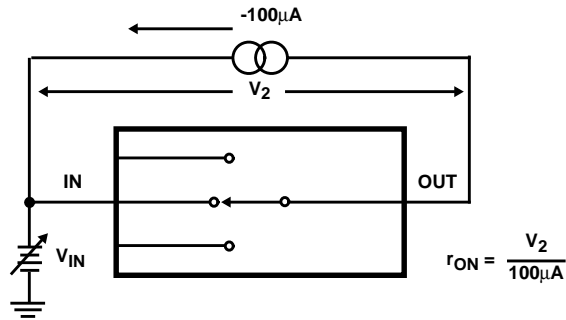


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

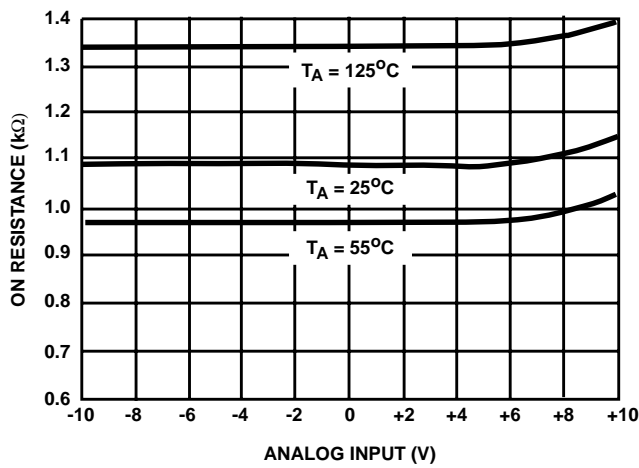


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

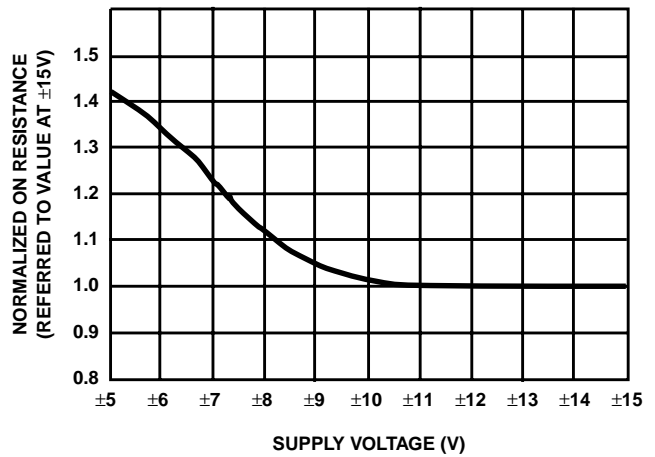


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

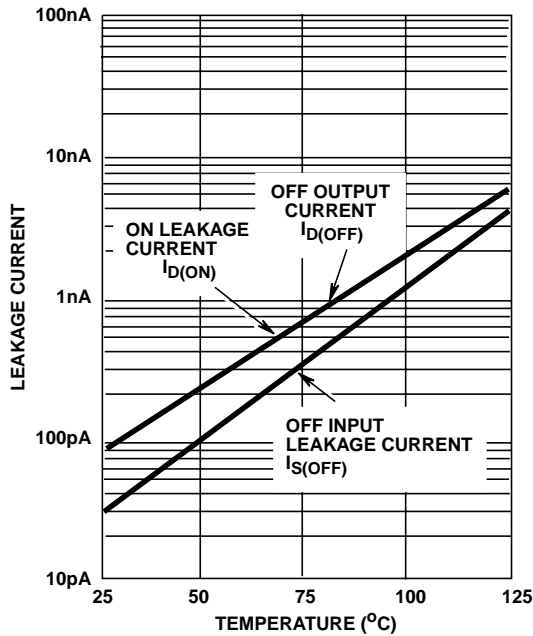


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

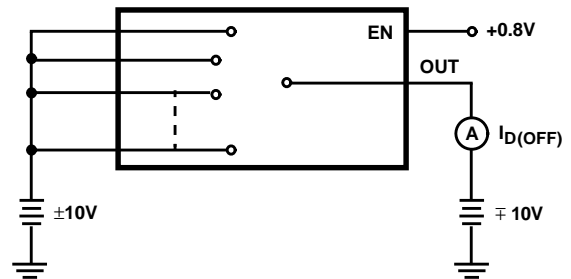


FIGURE 2B.  $I_{D(OFF)}$  TEST CIRCUIT



**Typical Performance Curves**  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = +4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$ ,  $V_{\text{REF}} = \text{Open}$ , Unless Otherwise Specified  
(Continued)

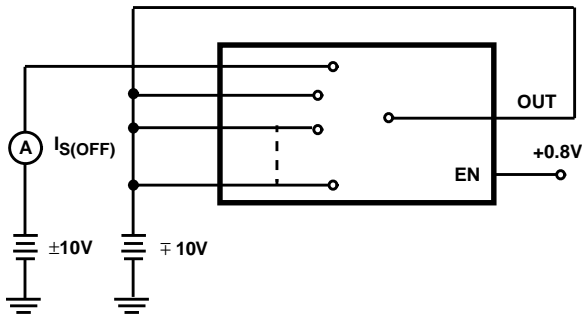


FIGURE 2C.  $I_{\text{S(OFF)}}$  TEST CIRCUIT

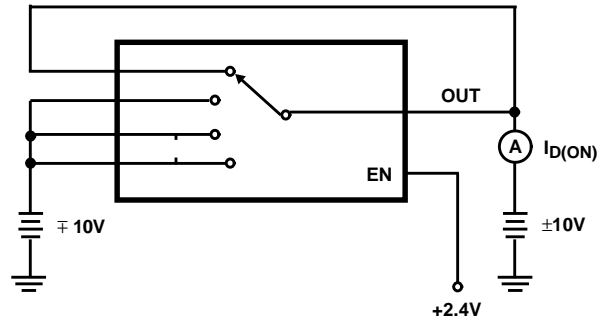


FIGURE 2D.  $I_{\text{D(ON)}}$  TEST CIRCUIT

NOTE:

- Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for  $I_{\text{D(OFF)}}$ : +10V/-10V and -10V/+10V.)

FIGURE 2. LEAKAGE CURRENT

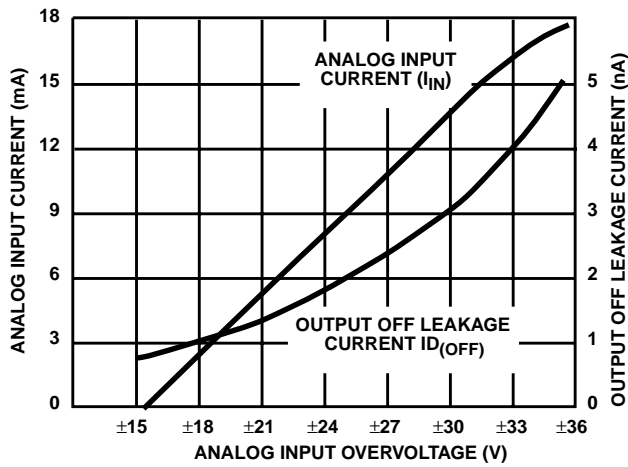


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVER-VOLTAGE

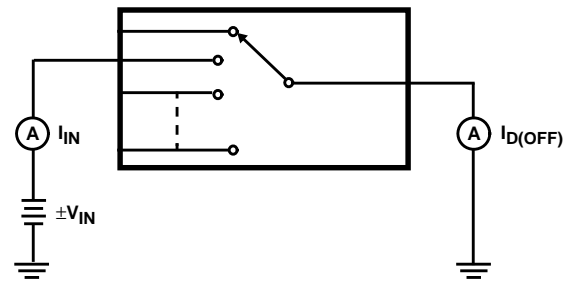


FIGURE 3B. ANALOG INPUT OVERVOLTAGE TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

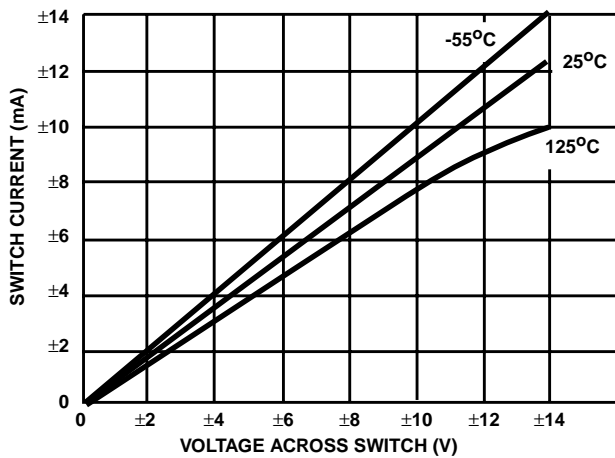


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

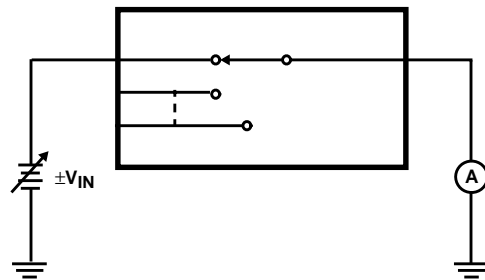


FIGURE 4B. ON CHANNEL CURRENT TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

**Typical Performance Curves**  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ ,  $V_{\text{AH}} = +4\text{V}$ ,  $V_{\text{AL}} = 0.8\text{V}$ ,  $V_{\text{REF}} = \text{Open}$ , Unless Otherwise Specified  
(Continued)

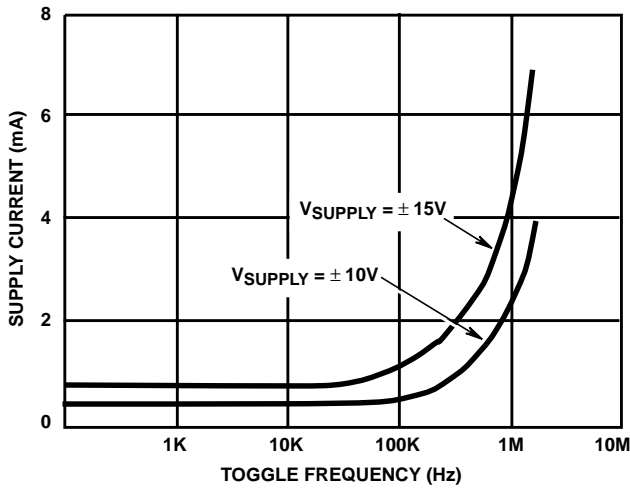
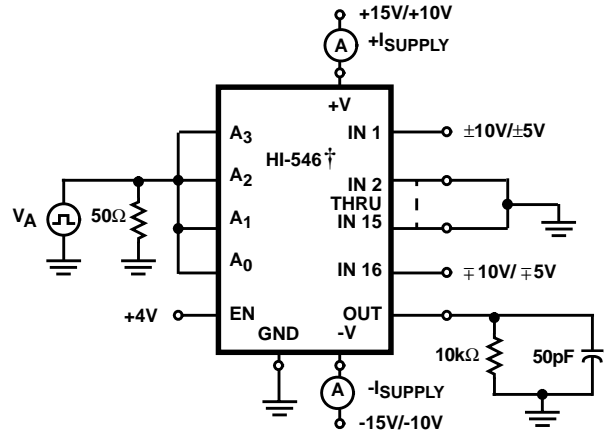


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



† Similar connection for HI-547/HI-548/HI-549.

FIGURE 5B. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. SUPPLY CURRENT

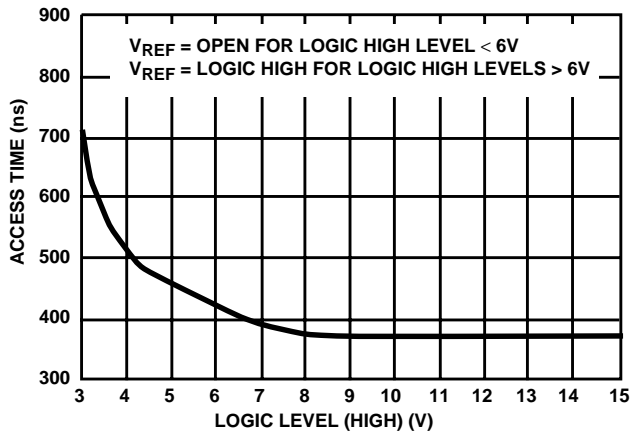
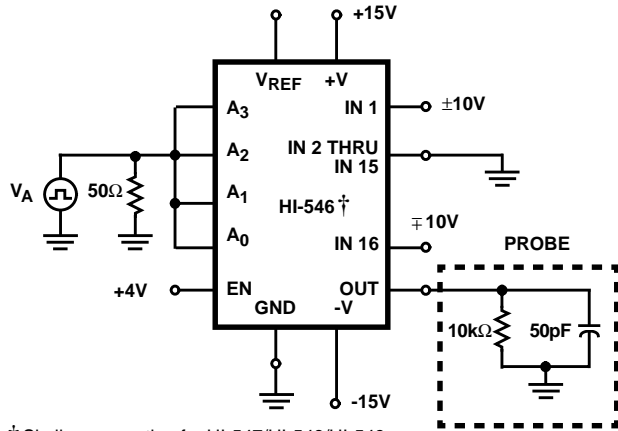


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



† Similar connection for HI-547/HI-548/HI-549.

FIGURE 6B. ACCESS TIME TEST CIRCUIT

FIGURE 6. ACCESS TIME

**Switching Waveforms**

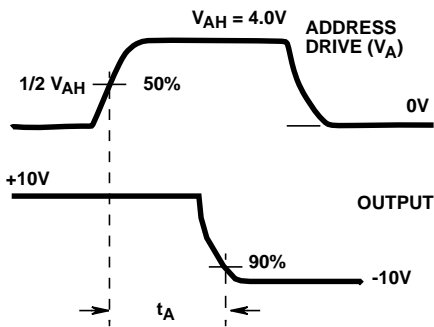


FIGURE 7A. ACCESS TIME MEASUREMENT

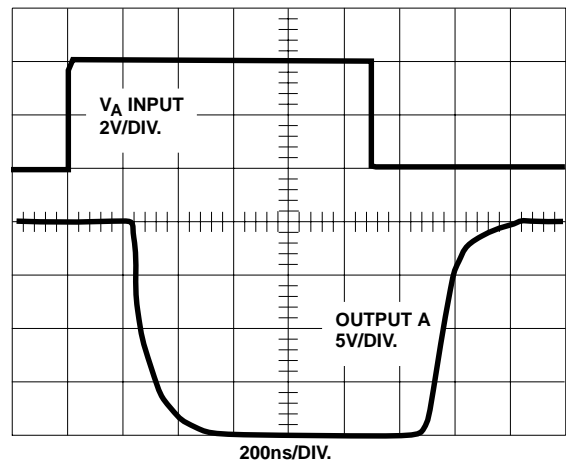
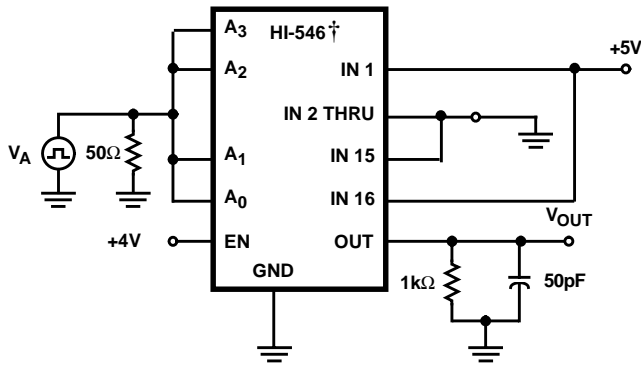


FIGURE 7B. ACCESS TIME WAVEFORMS

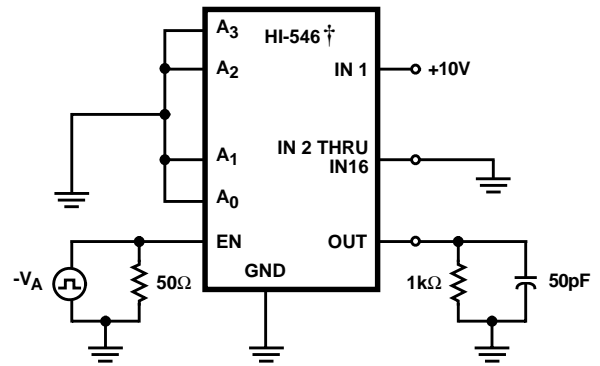
FIGURE 7. ACCESS TIME (Refer to Figure 6B for Test Circuit)

Switching Waveforms (Continued)



† Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. BREAK-BEFORE-MAKE DELAY TEST CIRCUIT



† Similar connection for HI-547/HI-548/HI-549

FIGURE 9A. ENABLE DELAY TEST CIRCUIT

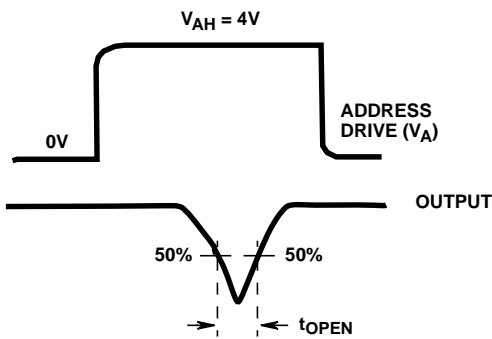


FIGURE 8B. BREAK-BEFORE-MAKE DELAY MEASUREMENT

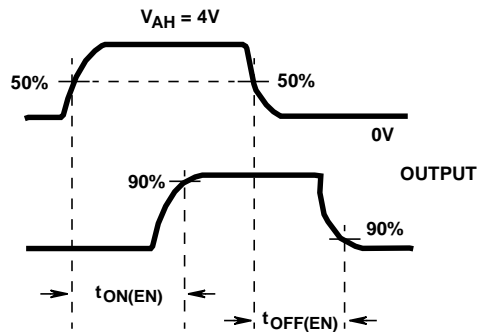


FIGURE 9B. ENABLE DELAY MEASUREMENTS

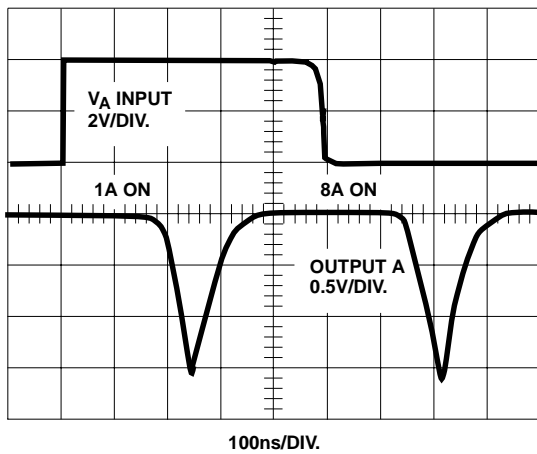


FIGURE 8C. BREAK-BEFORE-MAKE DELAY WAVEFORMS

FIGURE 8. BREAK-BEFORE-MAKE DELAY ( $t_{OPEN}$ )

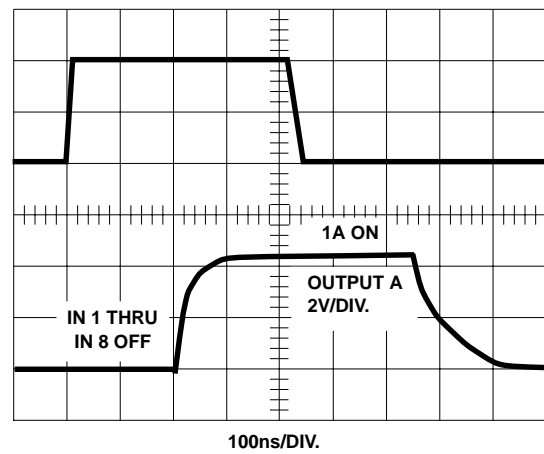


FIGURE 9C. ENABLE DELAY WAVEFORMS

FIGURE 9. ENABLE DELAY ( $t_{ON(EN)}$ ,  $t_{OFF(EN)}$ )

**HI-546, HI-547, HI-548, HI-549**

**Truth Tables**

**HI-546**

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

**HI-548**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

**HI-549**

A <sub>1</sub>	A <sub>0</sub>	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

**HI-547**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

# HI-546, HI-547, HI-548, HI-549

## Die Characteristics

### DIE DIMENSIONS:

83.9 mils x 159 mils x 19 mils

### METALLIZATION:

Type: CuAl

Thickness:  $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

### SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

### PASSIVATION:

Type: Nitride Over Silox

Nitride Thickness:  $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Silox Thickness:  $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

NOTE: The substrate appears resistive to the  $-V_{\text{SUPPLY}}$  terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at  $-V_{\text{SUPPLY}}$  potential.

### WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}^2$

### TRANSISTOR COUNT:

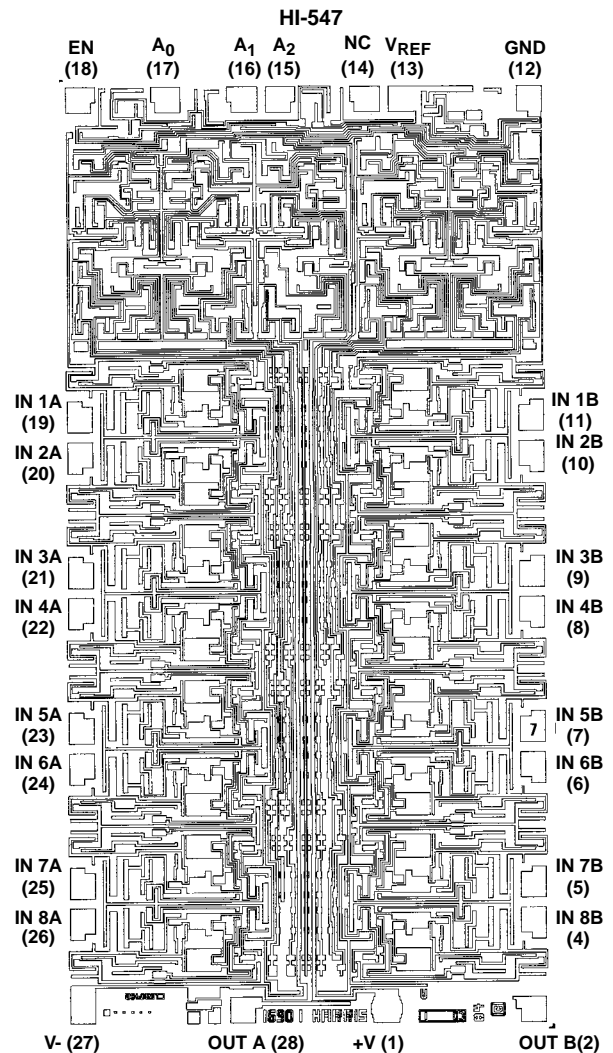
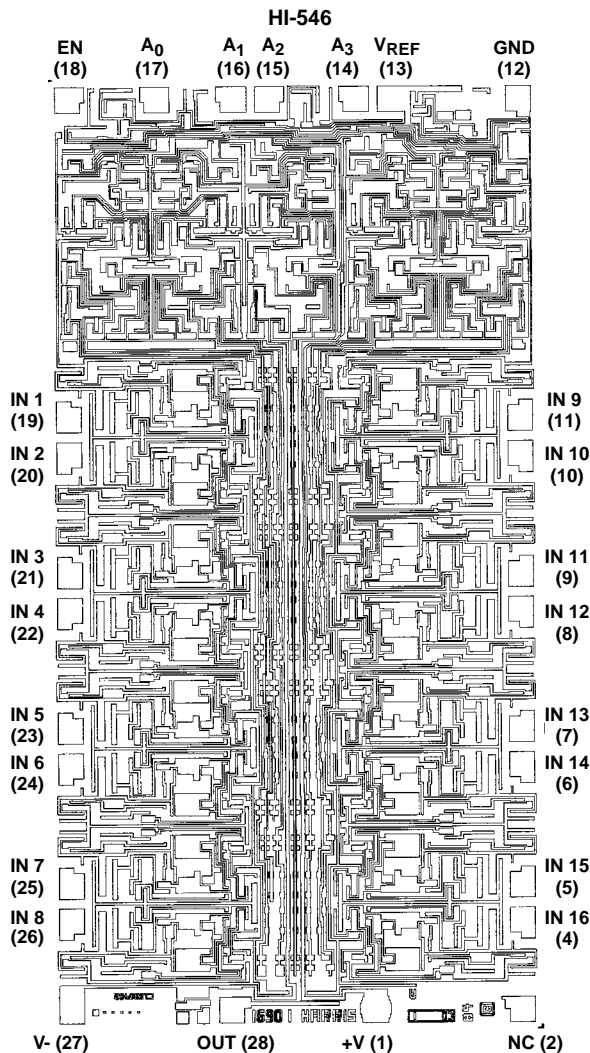
HI-546: 485

HI-547: 485

### PROCESS:

CMOS-DI

## Metallization Mask Layouts



# HI-546, HI-547, HI-548, HI-549

## Die Characteristics

### DIE DIMENSIONS:

83 mils x 108 mils x 19 mils

### METALLIZATION:

Type: CuAl

Thickness:  $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

### SUBSTRATE POTENTIAL (NOTE):

$-V_{\text{SUPPLY}}$

### PASSIVATION:

Type: Nitride Over Silox

Nitride Thickness:  $3.5\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Silox Thickness:  $12\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

NOTE: The substrate appears resistive to the  $-V_{\text{SUPPLY}}$  terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at  $-V_{\text{SUPPLY}}$  potential.

### WORST CASE CURRENT DENSITY:

$1.4 \times 10^5 \text{ A/cm}$

### TRANSISTOR COUNT:

HI-548: 253

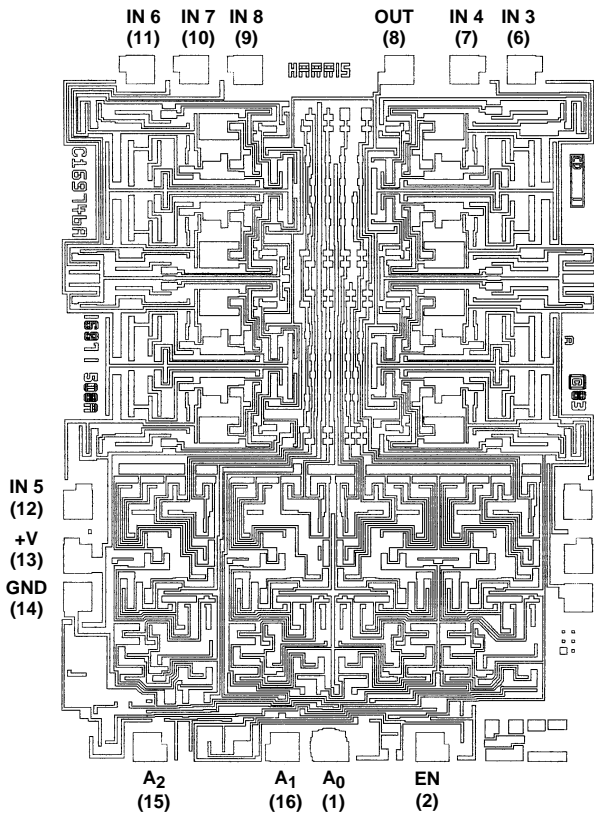
HI-549: 253

### PROCESS:

CMOS-DI

## Metallization Mask Layouts

HI-548



HI-549

